WHAT IS CLAIMED IS:

1. An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second spaced-apart doped region formed in the surface;

an isolation region disposed between said first and said second regions for electrically insulating said first and said second regions;

a plurality of layers overlying said first and said second doped regions, including a first and a second trench therein;

a third doped region formed in said first trench over said first doped region, and of a different conductivity type than said first doped region;

a fourth doped region formed in said second trench over said second doped region, and of a different conductivity type than said second doped region;

a first oxide layer proximate said third doped region; and

a second oxide layer proximate said fourth doped region.

2. The integrated circuit structure of claim 1 wherein the first doped region is a first source/drain region of a first MOSFET and the third doped region is a channel region of the first MOSFET, and wherein the third doped region is a first source/drain region of a second MOSFET and the fourth doped region is a channel region of the second MOSFET.

3. The integrated circuit structure of claim 2 wherein the first and the second MOSFETs form a complimentary MOSFET pair of transistors.

4. The integrated circuit structure of claim 1 wherein the isolation region comprises a trench of electrically insulating material disposed between the first and the second doped regions and a layer of electrically insulating material overlying the first and the second doped regions.

5. The integrated circuit structure of claim 1 wherein the material of the isolation region comprises an electrically insulating material.

6. The integrated circuit structure of claim 1 wherein the material of the isolation region comprises silicon dioxide.

7. The integrated circuit structure of claim 1 wherein one of the plurality of layers is removed to expose a portion over the third doped region in the first trench and a portion of the fourth doped region in the second trench, and wherein the first oxide layer is proximate said exposed portion of the third doped region, and wherein the second oxide layer is proximate said exposed portion of the fourth doped region.

8. The integrated circuit structure of claim 1 further comprising:

a fifth doped region overlying the first doped region and of the same conductivity type as the first doped region, wherein the first doped region is a first source/drain region of a first MOSFET, and wherein said fifth doped region is a second source/drain region of said first MOSFET, and wherein the third doped region is a channel region of said first MOSFET.

a sixth doped region overlying the second doped region of the same conductivity type as the second doped region, wherein the second doped region is a first source/drain region of a second MOSFET, and wherein said sixth doped region is a second source/drain region of said second MOSFET, and wherein the fourth doped region is a channel region of said second MOSFET; and wherein the first oxide layer is a gate oxide layer of said first MOSFET.

wherein the second oxide layer is a gate oxide layer of said second MOSFET.

9. The integrated circuit structure of claim 8 further comprising:

a first and a second conductive element adjacent the first and the second gate oxide layers, respectively, to control operation of the respective first and the second MOSFETs.

10. The integrated circuit structure of claim 9 wherein the first and the second conductive elements comprise polysilicon and operate as the gate for the first and the second MOSFETs, respectively.

11. The integrated circuit structure of claim 8 further comprising a third conductive element electrically connecting the first and the second source/drain regions.

12. The integrated circuit structure of claim 1 wherein at least one of the plurality of layers comprises a doped insulating layer for serving as a dopant source to diffuse dopants into the third and the fourth doped regions.

13. The integrated circuit structure of claim 12 wherein the third and the fourth doped regions each form a channel region, and wherein the dopants diffused from the doped insulating region form source/drain extensions within each of the channel regions.

14. An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second doped source/drain region formed in the major surface;

an isolation region disposed between said first and said second source/drain regions for electrically insulating said first and said second source/drain regions;

a plurality of layers overlying said first and said second source/drain regions, including a first and a second trench formed therein;

a first doped channel region formed in said first trench overlying said first source/drain region and having a different conductivity type than said first source/drain region;

a second doped channel region formed in said second trench overlying said second source/drain region and having a different conductivity type than said second source/drain region;

a third and a fourth doped spaced-apart source/drain region, wherein said third source/drain region is vertically aligned with said first channel region and said first source/drain region, and wherein said fourth source/drain region is vertically aligned with said second source/drain region and said second channel region, and wherein said third source/drain region is of the same conductivity type as the first source/drain region, and wherein said fourth source/drain region is of the some conductivity type as said second source/drain region;

a first oxide layer proximate said channel regions, and

a second oxide layer proximate said second channel region.

15. A method for fabricating a semiconductor structure having a plurality of field-effect transistors comprising:

forming a first device region, selected from the group consisting of a source region and a drain region of a first field-effect transistor on a semiconductor layer;

forming a second device region, selected from the group consisting of a source region and a drain region of a second field-effect transistor on the semiconductor layer;

forming an isolation region disposed between the first and the second device regions;

forming a first doped insulating layer over the first device region;

forming a second doped insulating layer overlying the first and the second device regions;

removing a portion of the second doped insulating layer overlying the first device region;

forming a sacrificial layer overlying the first and the second device regions;

forming a third doped insulating layer overlying the first device region;

forming a fourth doped insulating layer overlying the first and second device regions;

removing a portion of the fourth doped insulating layer overlying the first device region;

forming a first vertical trench extending downwardly from the upper surface of the third doped insulting layer to the upper surface of the first device region;

forming a second vertical trench extending downwardly from the upper surface of the fourth doped insulating layer to the upper surface of the second device region;

forming doped semiconductor material in the first and the second trenches, wherein the conductivity type of the doped semiconductor material in the first and the second trenches is opposite to the conductivity type of the first and the second underlying device regions, and wherein the doped semiconductor material in the first trench forms a channel region of a first field-effect transistor, and wherein the doped semiconductor material in the second trench forms a channel region of a second field-effect transistor ;

removing the sacrificial layer to expose a portion of the doped semiconductor material in the first and the second trenches;

forming first and second gate oxide material over the exposed portion of the doped semiconductor material in the first and the second trenches; and

forming first and second gates, wherein the first gate is electrical contact with the first gate oxide material, and wherein the second gate is an electrical contact with the second gate oxide material.

16. The method of claim 15 wherein dopants are diffused from the first, second, third and fourth doped insulating layers to form

extension regions within the channel region of the first and the second field-effect transistors.

17. The method of claim 15 wherein the step of forming the insulation region further comprises forming a trench between the first and the second device regions and forming and electrically insulating material within the trench.

18. The method of claim 15 wherein the material of the isolation region comprises silicon dioxide.

19. The method of claim 15 wherein the step of forming the isolation region further comprises forming a portion of the isolation region overlying the first and the second semiconductor regions.

20. The method of claim 15 wherein the material of the first and the third doped insulating layers comprises BTEOS, and wherein the material of the second and the fourth doped insulating layers comprises PTEOS, and wherein the material of the sacrificial layer comprises silicon dioxide.

21. The method of claim 15 wherein the steps of forming the first and the second doped insulating layers comprises;

forming an insulating layer overlying the first and the second device regions;

doping the portion of the insulating layer overlying the first device region with the dopant type of the first device region to form the first doped insulating layer; and

doping the portion of the insulating layer overlying the second device region with the dopant type of the second device region to form the second doped insulating layer.

22. The method of claim 21 wherein the step of doping the portion of the insulating layer overlying the first device region and the step of doping the portion of the insulating layer overlying the second

devise region comprises masking the undoped region and implanting the desired dopant type into the unmasked region.

23. The method of claim 15 wherein the steps of forming the third and the fourth doped insulating layers comprises;

forming an insulating layer overlying the first and the second device regions;

doping the portion of the insulating layer overlying the first device region with the dopant type of the first device region to form the third doped insulating layer; and

doping the portion of the insulating layer overlying the second device region with the dopant type of the second device region to form the fourth doped insulating layer.

24. The method of claim 23 wherein the step of doping the portion of the insulating layer overlying the first device region and the step of doping the portion of the insulating layer overlying the second device region comprise masking the undoped region and implanting the desired dopant type into the unmasked region.